Claims

[c1] 1.A graphics system comprising:
a dynamic-random-access memory (DRAM) for storing graphics data;
a static random-access memory (SRAM) for storing pixels in a frame buffer;
a first bus to the SRAM;
a second bus to the DRAM;
a refresh controller, coupled to the SRAM through the first bus, and coupled to the DRAM through the second bus, for reading pixels from the frame buffer for display to a display device;
a graphics engine, coupled to the SRAM through the first bus, and coupled to the DRAM through the second bus, for reading and writing graphics data; and
a dual-layer arbiter, receiving requests from the refresh controller to access the SRAM and requests from the graphics engine to access the DRAM, and also receiving requests from the refresh controller to access the DRAM and requests from the graphics engine to access the SRAM, the dual-layer arbiter allowing simultaneous access of the DRAM and SRAM when the refresh controller requests access of the SRAM and the graphics engine re-

quests access of the DRAM, but the dual-layer arbiter delaying access of the DRAM by the graphics engine when the refresh controller access the DRAM,
whereby the dual-layer arbiter allows simultaneous DRAM and SRAM access or arbitrated access of either the DRAM or the SRAM.

[c2] 2.The graphics system of claim 1 wherein the DRAM stores data as charges on capacitors that periodically require refreshing of the charges;
wherein the SRAM stores data as states of a bi-stable circuit.

[c3] 3.The graphics system of claim 1 wherein an access time for the SRAM is smaller than an access time for the DRAM.

[c4] 4.The graphics system of claim 3 further comprising:
a first mux, coupled between the refresh controller, the graphics engine, and the first bus, for connecting the refresh controller to the first bus in response to the dual-layer arbiter signaling that the refresh controller is granted access to the SRAM, but for connecting the graphics engine to the first bus in response to the dual-layer arbiter signaling that the graphics engine is granted access to the SRAM;
a second mux, coupled between the refresh controller,

the graphics engine, and the second bus, for connecting the refresh controller to the second bus in response to the dual-layer arbiter signaling that the refresh controller is granted access to the DRAM, but for connecting the graphics engine to the second bus in response to the dual-layer arbiter signaling that the graphics engine is granted access to the DRAM.

[c5] 5.The graphics system of claim 4 wherein the first bus can transfer data to the SRAM through the first mux at a same time that the second bus transfers data to the DRAM through the second mux.

[c6] 6.The graphics system of claim 5 wherein the first bus comprises address, data, and control signals for controlling access to the SRAM;
wherein the second bus comprises address, data, and control signals for controlling access to the DRAM.

[c7] 7.The graphics system of claim 4 further comprising:
a frame-buffer extension in the DRAM, the frame-buffer extension for storing pixels read by the refresh controller for larger frame buffers;
a buffer extension, in the SRAM, for storing graphics data read by the graphics engine.

[c8] 8.The graphics system of claim 4 further comprising:

a second graphics engine, coupled to the SRAM through the first bus, and coupled to the DRAM through the second bus, for reading and writing graphics data;
wherein the dual-layer arbiter further receives requests from the second graphics engine to access the DRAM, and requests from the second graphics engine to access the SRAM,
the dual-layer arbiter also allowing simultaneous access of the DRAM and SRAM when the refresh controller requests access of the SRAM and the second graphics engine requests access of the DRAM, but the dual-layer arbiter delaying access of the DRAM by the second graphics engine when the refresh controller access the DRAM,
wherein the first mux is further coupled to the second graphics engine, the first mux connecting the second graphics engine to the first bus in response to the dual-layer arbiter signaling that the second graphics engine is granted access to the SRAM;
wherein the second mux is further coupled to the second graphics engine, the second mux connecting the second graphics engine to the second bus in response to the dual-layer arbiter signaling that the second graphics engine is granted access to the SRAM.

[c9] 9.The graphics system of claim 8 wherein the graphics engine is a video overlay engine or a 3-dimensional

graphics engine.

[c10] 10.A dual-layer arbitrated graphics system comprising:
a dynamic-random-access memory (DRAM) for storing graphics data;
a static random-access memory (SRAM) for storing display pixels in a frame buffer;
an SRAM bus for transferring data to and from the SRAM;
a DRAM bus for transferring data to and from the DRAM;
a refresh controller coupled to drive display pixels to a display;
a first overlay engine that manipulates graphics data;
a first mux, coupled to the SRAM bus, for selecting either the refresh controller or the first overlay engine for coupling to the SRAM bus in response to a first select signal;
a second mux, coupled to the DRAM bus, for selecting either the refresh controller or the first overlay engine for coupling to the DRAM bus in response to a second select signal; and
a dual-layer arbiter coupled to receive requests from the refresh controller and requests from the first overlay engine, for arbitrating access to the SRAM when both the refresh controller and the first overlay engine request access to the SRAM, and for arbitrating access to the DRAM when both the refresh controller and the first overlay engine request access to the DRAM, but for al-

lowing parallel access to both the SRAM and to the DRAM when the refresh controller and the first overlay engine request access to different memories;
wherein the dual-layer arbiter generates the first select signal to the first mux and the second select signal to the second mux in response to the dual-layer arbiter arbitrating access or allowing parallel access,
whereby parallel access to the SRAM and to the DRAM is allowed when arbitrating access is not required by requests.

[c11] 11.The dual-layer arbitrated graphics system of claim 10 wherein the dual-layer arbiter arbitrates access using round-robin arbitration wherein the refresh controller and the first overlay engine are given equal priority for accessing the SRAM or the DRAM, or using priority arbitration wherein the refresh controller is given higher priority than the first overlay engine for accessing the SRAM or the DRAM.

[c12] 12.The dual-layer arbitrated graphics system of claim 11 further comprising:
a refresh controller request signal, generated by the refresh controller and sent to the dual-layer arbiter, for requesting access to the SRAM or to the DRAM by the refresh controller 20;
a refresh controller type signal, generated by the refresh

controller and sent to the dual-layer arbiter, for indicating when access to the SRAM is requested or when access to the DRAM is requested;
a first overlay engine request signal, generated by the first overlay engine and sent to the dual-layer arbiter, for requesting access to the SRAM or to the DRAM by the first overlay engine;
a first overlay engine type signal, generated by the first overlay engine and sent to the dual-layer arbiter, for indicating when access to the SRAM is requested or when access to the DRAM is requested.

[c13] 13.The dual-layer arbitrated graphics system of claim 12 further comprising:
a refresh controller grant signal, generated by the dual-layer arbiter and sent to the refresh controller, to indicate that the refresh controller may access a requested memory;
a first overlay engine grant signal, generated by the dual-layer arbiter and sent to the first overlay engine, to indicate that the first overlay engine may access a requested memory.

[c14] 14.The dual-layer arbitrated graphics system of claim 11 further comprising:
a second overlay engine, coupled to the first mux and to the second mux, for manipulating the graphics data;

wherein the first select signal further indicates when the second overlay engine is granted access to the SRAM by the dual-layer arbiter;
wherein the second select signal further indicates when the second overlay engine is granted access to the DRAM by the dual-layer arbiter.

[c15] 15.A dual-memory arbitrated graphics sub-system comprising:
dynamic-random-access memory (DRAM) means for storing graphics data;
static random-access memory (SRAM) means for storing display pixels in a frame buffer;
refresh controller means for reading the display pixels from the frame buffer and writing the display pixels to a display during a screen refresh;
first overlay engine means for processing the graphics data to generate display pixels or intermediate graphics data;
second overlay engine means for processing the graphics data to generate display pixels or intermediate graphics data;
arbiter means, receiving first requests for access of the SRAM means from the refresh controller means, the first overlay engine means, or the second overlay engine means, and receiving second requests for access of the

DRAM means from the refresh controller means, the first overlay engine means, or the second overlay engine means, for arbitrating among the first requests when received at a same time period to generate a first grant to a first winning requestor, and for arbitrating among the second requests when received at a same time period to generate a second grant to a second winning requestor, the arbiter means allowing simultaneous access of the SRAM means by the first winning requestor and the DRAM means by the second winning requestor;

first bus means for transferring address and data to the SRAM means;

second bus means for transferring address and data to the DRAM means;

first selector means, coupled to the first bus means, for selecting the refresh controller means, the first overlay engine means, or the second overlay engine means for connection to the first bus means in response to an indication of the first winning requestor from the arbiter means; and

second selector means, coupled to the second bus means, for selecting the refresh controller means, the first overlay engine means, or the second overlay engine means for connection to the second bus means in response to an indication of the second winning requestor from the arbiter means, whereby three requestors are arbitrated for access of two memories.

[c16] 16.The dual-memory arbitrated graphics sub-system of claim 15
wherein the first bus means is further for transferring control signals to the SRAM means;
wherein the second bus means is further for transferring control signals to the DRAM means;
wherein the first bus means and the second bus means differ in control signals and width of address.

[c17] 17.The dual-memory arbitrated graphics sub-system of claim 16 wherein the DRAM means is further for storing extension pixels in an extended frame buffer read by the refresh controller means.

[c18] 18.The dual-memory arbitrated graphics sub-system of claim 17 wherein the SRAM means is further for storing extension graphics data read by the first and second overlay engine means.

[c19] 19.The dual-memory arbitrated graphics sub-system of claim 15 wherein the arbiter means further comprises:
first round-robin means for alternately selecting as the first winning requestor the refresh controller means, the first overlay engine means, or the second overlay engine

means; and

second round-robin means for alternately selecting as the second winning requestor the refresh controller means, the first overlay engine means, or the second overlay engine means.

[c20] 20.The dual-memory arbitrated graphics sub-system of claim 15 wherein the arbiter means further comprises: priority means for selecting the refresh controller means as the first winning requestor when the first overlay engine means or the second overlay engine means also generates a first request during the same time period.